

## ECS Configuration Change Request

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Page(s)

<b>1. Originator</b> Robert Cole	<b>2. Log Date:</b> 5/16/02	<b>3. CCR #:</b> 02-0408	<b>4. Rev:</b>	<b>5. Tel:</b> 301-925-0799	<b>6. Rm #:</b> 2110C	<b>7. Dept.</b> SE/HW
<b>8. CCR Title:</b> Install new LaRC PDPS platform						
<b>9. Originator Signature/Date</b> Robert Cole /s/ 5/16/02			<b>10. Class</b> II	<b>11. Type:</b> CCR	<b>12. Need Date:</b> 5/31/02	
<b>13. Office Manager Signature/Date</b>			<b>14. Category of Change:</b> Update ECS Baseline Doc.		<b>15. Priority:</b> (If "Emergency" fill in Block 27). Routine	
<b>16. Documentation/Drawings Impacted:</b> see next page			<b>17. Schedule Impact:</b>		<b>18. CI(s) Affected:</b> SPRHW	
<b>19. Release Affected by this Change:</b> 6A		<b>20. Date due to Customer:</b>		<b>21. Estimated Cost:</b> None - Under 100K		
<b>22. Source Reference:</b> <input type="checkbox"/> NCR (attach) <input type="checkbox"/> Action Item <input type="checkbox"/> Tech Ref. <input type="checkbox"/> GSFC <input type="checkbox"/> Other:						
<b>23. Problem: (use additional Sheets if necessary)</b> A new E4000 platform has been obtained to serve as the new PDPS (consolidated planning/queueing) server for LaRC. This platform is the former g0dis01 and has been configured with 4x400 MHz CPUs and 2 GB RAM.  This platform needs to be installed at LaRC for Solaris transition						
<b>24. Proposed Solution: (use additional sheets if necessary)</b> see next page						
<b>25. Alternate Solution: (use additional sheets if necessary)</b>						
<b>26. Consequences if Change(s) are not approved: (use additional sheets if necessary)</b>						
<b>27. Justification for Emergency (If Block 15 is "Emergency"):</b>						
<b>28. Site(s) Affected:</b> <input type="checkbox"/> EDF <input type="checkbox"/> PVC <input type="checkbox"/> VATC <input type="checkbox"/> EDC <input type="checkbox"/> GSFC <input checked="" type="checkbox"/> LaRC <input type="checkbox"/> NSIDC <input type="checkbox"/> SMC <input type="checkbox"/> AK <input type="checkbox"/> JPL <input type="checkbox"/> EOC <input type="checkbox"/> IDG Test Cell <input type="checkbox"/> Other						
<b>29. Board Comments:</b>			<b>30. Work Assigned To:</b>		<b>31. CCR Closed Date:</b>	
<b>32. EDF/SCDV CCB Chair (Sign/Date):</b>		<b>Disposition:</b> Approved App/Com. Disapproved Withdraw Fwd/ESDIS ERB Fwd/ECS				
<b>33. M&amp;O CCB Chair (Sign/Date):</b> Gary Gavigan /s/ 5/21/02		<b>Disposition:</b> <span style="border: 1px solid red; color: red;">Approved</span> App/Com. Disapproved Withdraw Fwd/ESDIS ERB Fwd/ECS				
<b>34. ECS CCB Chair (Sign/Date):</b>		<b>Disposition:</b> Approved App/Com. Disapproved Withdraw Fwd/ESDIS ERB Fwd/ESDIS				

TDx: TD=Technical Document, x=Site Identifier, nnn=Document ID within a document series

## ADDITIONAL SHEET

**CCR #:**                      **Rev:**                      **Originator:**

**Telephone:**                      **Office:**

**Title of Change:**

**Note:**

This CCR documents the installation of the machine only. Consequently, updates to hardware software map will be made via the Solaris 8 PSR.

**Affected drawings:**

920-TDL-001, update included  
922-TDL-014, update included  
921-TDL-002, action item for completion after transition  
921-TDL-003, action item for completion after transition  
920-TDL-004, action item for completion after transition  
920-TDL-005, action item for completion after transition

**Proposed Solution:**

Install E4000 (EIN 1876) at LaRC as I0sps11 with multipack EIN 4967. This name will be temporary for the duration of Solaris transition after which it will revert back to I0sps03 (existing queuing server name). Use temporary IP address 198.118.219.200 and connect to port 4/42 on the Catalyst switch.

After transition, remove the 2 2x400 MHz CPU board from slot 5 of I0pls01 and install in new PDPS platform. Also remove the 2x400 MHz CPU board in slot 7 and install in new platform, however, remove the second bank of DIMMs from this board and install in the existing CPU board which has 2 CPUs and no memory.

Final CPU board configuration for new platform: 8x400 MHz, 5 GB mem (2 GB in one bank on one board, 1 GB in one bank on each of the other 3 boards)